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| APPLICATION NO. | FILING DATE | FIRST NAMED INVENTOR | ATTORNEY DOCKET NO. | CONFIRMATION NO. |
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| 09/834,276 | 04/12/2001 | Roger Lewis | H26651 | 4922 |

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| EXAMINER |
|---|
| SHAPIRO, LEONID |

| ART UNIT | PAPER NUMBER |
|---|---|
| 2673 | 7 |

DATE MAILED: 09/12/2003

Please find below and/or attached an Office communication concerning this application or proceeding.

| Office Action Summary | Application No. | Applicant(s) | |
|---|---|---|---|
| | 09/834,276 | LEWIS, ROGER | |
| | Examiner | Art Unit | |
| | Leonid Shapiro | 2673 | |

*-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --*

**Period for Reply**

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

**Status**

1)☒ Responsive to communication(s) filed on *04 August 2003* .

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

**Disposition of Claims**

4)☒ Claim(s) *1-12, 14-19 and 21-23* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-12, 14-19 and 21-23* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

**Application Papers**

9)☒ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *12 April 2001* is/are: a)☐ accepted or b)☒ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

**Priority under 35 U.S.C. §§ 119 and 120**

13)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

**Attachment(s)**

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449) Paper No(s) *1* .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: .

***Information Disclosure Statement***

1. A copy of the 1449 Form filed on 04-12-01 was considered and attached with this communication.

***Drawings***

2. The drawings were received and approved on 08-04-03. These drawings are Figs.1 and 10.

3. The drawings are objected to under 37 CFR 1.83(a). The drawings must show every feature of the invention specified in the claims. Therefore, the "hardware based pulse width modulator" must be shown or the feature(s) canceled from the claim(s). No new matter should be entered.

A proposed drawing correction or corrected drawings are required in reply to the Office action to avoid abandonment of the application. The objection to the drawings will not be held in abeyance.

***Specification***

4. The disclosure is objected to because of the following informalities:

On page 4, Lines 9-11 the definition of PWM duty cycle contradicted to Equation (1) on page 6.

On page 9, Line 4 mentioned "waveform" in Fig. 5B. Fig. 5B is a diagram without "waveform'.

On page 10, Line 3, mentioned formula : N= log2 K. In Fig. 8, step 700, 702, 704 it is N+ log2 K.

Appropriate correction is required.

### *Claim Rejections - 35 USC § 112*

The following is a quotation of the first paragraph of 35 U.S.C. 112:

> The specification shall contain a written description of the invention, and of the manner and process of making and using it, in such full, clear, concise, and exact terms as to enable any person skilled in the art to which it pertains, or with which it is most nearly connected, to make and use the same and shall set forth the best mode contemplated by the inventor of carrying out his invention.

5. Claims 21-23 rejected under 35 U.S.C. 112, first paragraph, as failing to comply with the written description requirement. The claim(s) contains subject matter which was not described in the specification in such a way as to reasonably convey to one skilled in the relevant art that the inventor(s), at the time the application was filed, had possession of the claimed invention. The newly introduced limitation " a hardware based pulse width modulator" is not defined in the specification.

### *Claim Rejections - 35 USC § 103*

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

6. Claims 1-2, 4-6, 8-9,11-12,14-17,19 are rejected under 35 U.S.C. 103(a) as being unpatentable over Zuraski et al. (US Patent No. 5,589,805) in view of Akiko (JP 04-096417).

As to claim 1, Zuraski et al. teaches a method for pulse width modulation comprising the steps of: providing a pulse width modulator having n (6) bits of resolution (See Figs. 1A-B, 3,

items Tc,T1,T2,17, in description See Col.3, Lines 32-35, from Col. 3, Line 63 to Col. 4, Line 9 and Col. 5, Lines 1-8) and nominal time period Pn (Tpwm) (See Figs. 1A-B, 3, items Tpwm, 17, in description See Col.3, Lines 32-35, from Col. 3, Line 63 to Col. 4, Line 9 and Col. 5, Lines 1-8); supplying an additional timer to generate K (2) associated states and having period Pt (T1 or T2) (See Fig. 3,1A-B, items T1, T2, 17, in description See Col. 5, Lines 9-27); associating a modulator output value with each one of K states (See Figs. 1A-B, 3, items Tc,T1,T2,17, in description See Col. 5, Lines 9-27).

Zuraski et al. does not show an additional timer to generate K associated states , wherein K is grater than 2 and establishing a pulse width modulation update interval K*Pt

Akiko teaches a timer with an 8-bit resolution is used and PWM output having a resolution of 10-bits (See Figs. 2, 5, items 1-2, in Detailed Description See Page 1 , last paragraph and Page 3, 1st paragraph).

It would have been obvious to one of ordinary skill in the art at the time of the invention to use timer with K greater than 2 as shown by Akiko in the Zuraski et al. method and apparatus and multiply number of the states of the counter by the period of the resolution to obtain the update rate in order to enhance the output resolution of PWM system as an obvious variation in a method to improve PWM system resolution (See Col. 1, Lines 34-46 in the Zuraski et al. reference and Purpose in Akiko reference).

As to claim 5, Zuraski et al. teaches a method for improving the resolution of an n (6) bit pulse width modulator (See Figs. 1A-B, 3, items Tpwm,17, in description See Col.3, Lines 32-35, from Col. 3, Line 63 to Col. 4, Line 9 and Col. 5, Lines 1-8) having a nominal time period Pn (Tpwm) (See Figs. 1A, 3, items Tc, 17, in description See Col.3, Lines 32-35, from Col. 3, Line

63 to Col. 4, Line 9 and Col. 5, Lines 1-8), comprising the steps of : supplying an additional timer having K (2) associated states and timer period Pt (T1 or T2) (See Fig. 3,1A-B, items T1,T2, 17, in description See Col.5, Lines 9-27); associating a modulator output value with each one of K states (See Figs. 1A-B, 3, items Tc,T1,T2,17, in description See Col. 5, Lines 9-27).

Zuraski et al. does not show an additional timer to generate K associated states , wherein K is grater than 2 and outputting a pulse according to modulator output value during each time period Pn occurring within timer period Pt during each one of K timer states, whereby the resolution of n bit pulse width modulator substantially equals n+ log2 (K).

Akiko teaches a timer with an 8-bit resolution is used and PWM output having a resolution of 10-bits (n+8) (See Figs. 2, 5, items 1-2, in Detailed Description See Page 1, last paragraph and Page 3, first three paragraphs).

It would have been obvious to one of ordinary skill in the art at the time of the invention to use timer with K greater than 2 and add resolution of n bit pulse width modulator to 8 bits of resolution of timer as shown by Akiko in the Zuraski et al. method and apparatus in order to improve PWM system resolution (See Col. 1, Lines 34-46 in the Zuraski et al. reference and Purpose in Akiko reference).

As to claim 14, Zuraski et al. teaches an apparatus for pulse width modulation comprising: n(6) bit pulse width modulation (See Figs. 1A-B, 3, items Tc,T1, T2, 17, in description See Col.3, Lines 32-35, from Col. 3, Line 63 to Col. 4, Line 9 and Col. 5, Lines 1-8) having a nominal time period Pn (Tpwm) (See Figs. 1A, 3, items Tpwm, 17, in description See Col.3, Lines 32-35, from Col. 3, Line 63 to Col. 4, Line 9 and Col. 5, Lines 1-8), a timer to generate K (2) associated states and having period Pt (T1 or T2) (See Fig. 3,1A-B, items T1,T2,

17, in description See Col.5, Lines 9-27); a computing device for assigning a modulator output value to each of K states (See Figs. 5-6, items 503, 601, in description See Col. 8, Lines 12-29).

Zuraski et al. does not show an additional timer to generate K associated states , wherein K is grater than 2 and outputting a pulse according to modulator output value during each time period Pn occurring within timer period Pt during each one of K timer states, whereby the resolution of n bit pulse width modulator substantially equals n+ log2 (K).

Akiko teaches a timer with an 8-bit resolution is used and PWM output having a resolution of 10-bits (n+8) (See Figs. 2, 5, items 1-2, in Detailed Description See Page 1, last paragraph and Page 3, first three paragraphs).

It would have been obvious to one of ordinary skill in the art at the time of the invention to use timer with K greater than 2 and add resolution of n bit pulse width modulator to 8 bits of resolution of timer as shown by Akiko in the Zuraski et al. method and apparatus in order to improve PWM system resolution (See Col. 1, Lines 34-46 in the Zuraski et al. reference and Purpose in Akiko reference).

As to claim 19, Zuraski et al. teaches an apparatus improving the resolution of n(6) bit pulse width modulator (See Figs. 1A-B, 3, items Tc,T1, T2, 17, in description See Col.3, Lines 32-35, from Col. 3, Line 63 to Col. 4, Line 9 and Col. 5, Lines 1-8) having a nominal time period Pn (Tpwm) (See Figs. 1A, 3, items Tpwm, 17, in description See Col.3, Lines 32-35, from Col. 3, Line 63 to Col. 4, Line 9 and Col. 5, Lines 1-8), the apparatus comprising: a timer to generate K (2) associated states and having period Pt (T1 or T2) (See Fig. 3,1A-B, items T1,T2, 17, in description See Col.5, Lines 9-27); a computing device for assigning a modulator output value to each of K states (See Figs. 5-6, items 503, 601, in description See Col. 8, Lines 12-29).

Zuraski et al. does not show an additional timer to generate K associated states , wherein K is grater than 2 and outputting a pulse according to modulator output value during each time period Pn occurring within timer period Pt during each one of K timer states, whereby the resolution of n bit pulse width modulator substantially equals n+ log2 (K).

Akiko teaches a timer with an 8-bit resolution is used and PWM output having a resolution of 10-bits (n+8) (See Figs. 2, 5, items 1-2, in Detailed Description See Page 1, last paragraph and Page 3, first three paragraphs).

It would have been obvious to one of ordinary skill in the art at the time of the invention to use timer with K greater than 2 and add resolution of n bit pulse width modulator to 8 bits of resolution of timer as shown by Akiko in the Zuraski et al. method and apparatus in order to improve PWM system resolution (See Col. 1, Lines 34-46 in the Zuraski et al. reference and Purpose in Aiko reference).

As to claims 11-12, Zuraski et al. teaches a computer program product for pulse width modulation comprising: a computer readable storage medium having computer readable program code embedded in medium (See Figs. 3-5, items 10, 501-509, in description See Col. 7, Lines 5-20), computer readable program code means having: a first computer instruction means for associating K timer states a period Pt (See Fig. 5, items 507-509, in description See from Col. 7, Line 300 to Col. 8, Line 10); à second computer instruction means for reading a commanded pulse width modulation cycle (See Fig. 5, item 501, in description See Col. 7, Lines 22-30); a third computer instruction means for assigning a n bit modulator output with each one of K states according to the duty cycle (See Figs. 5-6, items 503, 601, in description See Col. 8, Lines 12-29).

Zuraski et al. does not show an additional timer to generate K associated states , wherein K is grater than 2.

Akiko teaches a timer with an 8-bit resolution is used and PWM output having a resolution of 10-bits (See Figs. 2, 5, items 1-2, in Detailed Description See Page 1 , last paragraph and Page 3, 1st paragraph).

It would have been obvious to one of ordinary skill in the art at the time of the invention to use timer with K greater than 2 as shown by Akiko in the Zuraski et al. method and apparatus in order to improve PWM system resolution (See Col. 1, Lines 34-46 in the Zuraski et al. reference and Purpose in Akiko reference).

As to claims 2,6,16, Zuraski et al. teaches Pt is an integer multiple of Pn, since Tc and Tpwm are both derived from microprocessor clock (See Fig. 3, item 17, in description See Col. 3, Lines 33-40).

As to claims 4,8 Zuraski et al. teaches conventional case where Pt=Pn (T1=Tpwm without internal microprocessor timers) (See Figs. 1A-B, 3, in description See Col. 5, Lines 9-27).

As to claims 9,17, Zuraski et al. teaches Pt (T1) >> Pn (Tpwm) (See Figs.1A-B, items Tpwm and Tc, T1, T2).

Zuraski et al. does not show Pt is other than integer multiple of Pn. It would have been obvious to one of ordinary skill in the art at the time of the invention to use external clock to the timers of the microprocessor to have Pt other than integer multiple of Pn in the Zuraski et al. method.

As to claim 15, Zuraski et al. teaches timers are included within computing device (See Fig. 3, item 10, in description See Col. 3, Lines 30-36).

7. Claims 3, 7, 10, 18 are rejected under 35 U.S.C. 103(a) as being unpatentable Zuraski et al. and Akiko as aforementioned in claims 1, 5, 14 in view of Shibuya et al. (US Patent No. 6,191,868 B10)

Zuraski et al. and Akiko do not show pulse width modulator includes an overflow bit.

Shibuya et al. teaches to truncate the overflow bit (See Fig. 2, item 17, in description See Col. 4, Lines 58-65). It would have been obvious to one of ordinary skill in the art at the time of the invention to implement the overflow approach as shown by Shibuya et al. in the Zuraski et al. and Akiko method and apparatus in order to enhance the output resolution of PWM system (See Col. 1, Lines 34-46 in the Zuraski et al. reference).

***Response to Amendment***

8. Applicant's arguments filed on 08-04-03 with respect to claims 1-12, 14-19 have been considered but are moot in view of the new ground(s) of rejection.

***Conclusion***

9. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

***Telephone inquire***

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Leonid Shapiro whose telephone number is 703-305-5661. The examiner can normally be reached on 8 a.m. to 5 p.m..

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Bipin Shalwala can be reached on 703-305-4938. The fax phone number for the organization where this application or proceeding is assigned is (703) 872-9306.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is 703-305-4750.

ls

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